

**C. REMARKS**

Reconsideration and allowance are requested in view of the foregoing amendments and the following remarks.

**35 U.S.C. § 103(a) Rejection**

Claims 77-90 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,040,291 to Janisiewicz et al. ("Janisiewicz") in view of U.S. Patent No. 5,805,421 to Livengood et al. ("Livengood"), and in further view of U.S. Patent No. 4,675,993 to Harada ("Harada") and U.S. Patent No. 5,084,962 to Takahashi et al. ("Takahashi"). Applicants respectfully traverse this rejection.

In the present Office action, the Examiner admits that Janisiewicz fails to teach "fiducial markers and an optical fiducial marker detector and a controller"<sup>1</sup> yet alleges that it would have been obvious "to modify Janisiewicz by providing fiducial markers and comparing steps, as taught by Livengood, for the purpose of correctly positioning components on printed circuit boards."<sup>2</sup> The Examiner also alleges that it would have been obvious "to modify Janisiewicz by providing a printed fiducial marker detector, comparing steps and a controller, as taught by Harada, for the purpose of correctly positioning components on printed circuit boards."<sup>3</sup> The Examiner further alleges that it would have been obvious "to modify Janisiewicz by providing an optical fiducial maker (sic), as taught by Takahashi, for the purpose of determining a component's exact position."<sup>4</sup> Applicants submit, however, that Livengood, Harada, and Takahashi, alone or in combination, fail to remedy the admitted deficiencies of Janisiewicz for at least the following reasons.

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<sup>1</sup> See Office action, p.2.

<sup>2</sup> Id. at p. 3.

<sup>3</sup> Id.

<sup>4</sup> Id.

While Livengood does disclose chip fiducials 35, there is no teaching or suggestion to use such chip fiducials 35 for *correctly positioning components*. To the contrary, Livengood relates to testing "[o]nce a newly designed integrated circuit (IC) *has been formed* on a silicon substrate"<sup>5</sup> to obtain important electrical data from the IC, such as, voltage levels, timing information, current levels, and thermal information.<sup>6</sup> In particular, Livengood characterizes its principal of operation as follows:

There are two relatively distinct aspects to the present invention which work together in order to allow a practitioner to probe an IC device (or "chip") from the bottom of the semiconductor substrate upon which the IC is formed. First, a method is proposed which allows virtual navigation through the circuitry of the chip from the bottom of the chip. The navigational method offered herein permits a practitioner to accurately determine a point on the bottom of the chip residing directly below a corresponding point in the circuitry on top of the chip which the practitioner desires to probe (the probe point). Second, various techniques are offered herein whereby a hole is etched through the bottom of the chip in order to allow probing of the probe point.<sup>7</sup>

Livengood explicitly states that the package fiducials 33 are necessary to locate the chip fiducials 35. Namely, the approximate locations of the chip fiducials 35 are determined by using the packaging fiducials 33 for guidance (e.g., x-y coordinate system).<sup>8</sup> At the approximate locations, alignment holes 34 are etched through the bottom of chip 40 to expose the chip fiducials 35.<sup>9</sup> Because the packaging fiducials 33 needed to locate the chip fiducials 35 are formed on the substrate 43, it is clear that the chip 40 must have been positioned prior to exposure of the chip fiducials 35. Therefore, the chip fiducials 35 in Livengood must be used for a purpose other than for positioning the chip 40 on the package substrate 43.

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<sup>5</sup> See Livengood at col. 1, ll. 15-17 (emphasis added).

<sup>6</sup> *Id.* at col. 1, ll. 15-40.

<sup>7</sup> *Id.* at col. 4, ll. 18-30.

<sup>8</sup> *Id.* at col. 5, ll. 55+

<sup>9</sup> *Id.*

Indeed, once exposed, the chip fiducials 35 are used in conjunction with a circuit diagram to locate points on the bottom of the chip 40 which are directly below probe points in the circuitry on top of the chip 40.<sup>10</sup> Probe holes 52 are etched through a locally thinned region 45 of the silicon substrate 46 and through a portion of silicon dioxide layer 47 to allow electron-beam probing of interconnect lines 49 from the bottom of chip 40.<sup>11</sup>

According to Livengood, the chip fiducials 35 are used to locate probe points. This establishes both that the chip fiducials 35 are not used for positioning the chip 40 and that there would be no suggestion or motivation to do so. Namely, the principal of operation of Livengood is to allow testing via the probing points, which is possible only after the chip 40 has been positioned on the package substrate 43.

Clearly, there is no teaching or suggestion in Livengood to use the chip fiducials 35 for ***correctly positioning components***, as alleged by the Examiner. Applicants remind the Examiner that the Federal Circuit has explained repeatedly that to support an obvious rejection, the prior art must suggest not merely that modification of the prior art is possible, but rather that the exact modification at issue is desirable.<sup>12</sup>

Harada discloses a marker printed with magnetic ink at the center of the component.<sup>13</sup> According to Harada, a vacuum fastener having a magnetic sensor may attract the center of the component.<sup>14</sup> Harada is devoid, however, of any teaching or suggestion that the magnetic marker may indicate an orientation of a plurality of leads protruding from the component.

And, the newly cited reference Takahashi merely discloses "a second camera for picking up a picture of a positioning mark or a fiducial mark, e.g., a through-hole or the like, the

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<sup>10</sup> Id. at col.7, ll. 18-22.

<sup>11</sup> Id. at col. 8, ll. 40+

<sup>12</sup> See, e.g., *In re Laskowski*, 871 F.2d 115 (Fed. Cir. 1989) ("[T]he mere fact that the prior art could be so modified would not have made the modification obvious unless the prior art suggested the desirability of the modification."); *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990) (Although a prior art device "may be capable of being modified to run the way [that applicant's] apparatus is claimed, there must be some suggestion or motivation in the reference to do so.").

<sup>13</sup> See Harada, col. 6, ll. 15-23.

<sup>14</sup> Id.

positioning mark being previously applied onto a printed circuit board on the X-Y table."<sup>15</sup> There is no teaching of a fiducial mark on a component and, hence, no suggestion to use the camera to detect a fiducial mark on a component.

The Examiner is reminded that in order to establish such a *prima facie* case of obviousness, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings.<sup>16</sup> In addition, there must be a reasonable expectation of success.<sup>17</sup> Moreover, the prior art must teach or suggest all of the claim limitations.<sup>18</sup> Such teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure.<sup>19</sup>

Applicants submit that even if Livengood, Harada, and Takahashi could be combined with each other and with Janisiewicz, which Applicants do not admit, such combination still would fail to disclose all the elements of independent claims 77, 82 and 85. Furthermore, the devices described in Livengood, Harada, and Takahashi clearly operate on different principles and therefore cannot be combined without destroying the functionality of the corresponding devices. Moreover, there is no motivation or suggestion in the cited art for combining Livengood, Harada, and Takahashi with each other or with Janisiewicz.

For at least these reasons, Applicants submit that the outstanding grounds of rejections are based on impermissible hindsight reconstruction, using Applicants' claim as a template to reconstruct the claimed invention by picking and choosing isolated disclosures from the prior art.<sup>20</sup> The Examiner is required to do more than point to isolated disclosures of components from the prior art which are used separately or in other combinations; there must be some teaching, suggestion, or incentive to make the combination made by the inventor.<sup>21</sup>

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<sup>15</sup> See Takahashi, col. 1, ll. 56-59.

<sup>16</sup> See MPEP § 2143 citing *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

<sup>17</sup> *Id.*

<sup>18</sup> *Id.*

<sup>19</sup> *Id.*

<sup>20</sup> See *In re Fritch*, 972 F.2d 1260, 1266, 23 U.S.P.Q.2d 1780, 1784 (Fed. Cir. 1992).

<sup>21</sup> See *Northern Telecom, Inc. v. Datapoint Corp.*, 908 F.2d 931, 934, 15 U.S.P.Q.2d 1321, 1323 (Fed. Cir. 1990).

While Applicants disagree with the Examiner's grounds rejections, independent claims 77, 82, and 85 have been amended in order to expedite prosecution. In particular, Applicants have amended claim 77 to recite the fiducial marker on the retrieved component is visible for detection prior to placement of said retrieved component on the substrate and an optical fiducial marker detector oriented to detect the fiducial marker on said retrieved component prior to placement of said retrieved component on the substrate and generate alignment data for said retrieved component. Applicants have amended claim 82 to recite the fiducial marker on the retrieved component is visible for detection prior to placement of said retrieved component on a substrate and an optical fiducial marker detector oriented to detect the detectable location of the fiducial marker on the said retrieved component prior to placement of said retrieved component on a substrate and generate alignment data for said retrieved component. Applicants have amended claim 85 to recite the fiducial marker is visible for detection prior to placement of said retrieved component on a substrate and an optical marker detector oriented to detect the marker on the retrieved component prior to placement of said retrieved component on a substrate and generate alignment data that is indicative of the position of the marker within the transfer area.

Applicants submit that the prior art of record, including Janisiewicz, Livengood, Harada, and Takahashi, fails to teach or suggest all the elements of independent claims 77, 82, and 85. In addition, Applicants contend that the prior art of record fails to provide any suggestion or motivation to modify or combine reference teachings or of a reasonable expectation of success. Applicants submit, therefore, that claims 77, 82, and 85 are allowable for at least the reasons set forth above and that claims 78-81, 83, 84, and 86-90 are allowable by virtue of their dependency, as well as on their own merits.

**D. CONCLUSION**

Applicants submit this application is in condition for allowance and request favorable action in the form of a Notice of Allowance.

Respectfully submitted,

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A handwritten signature in cursive script, appearing to read "Robert V. Racunas, Jr.", is written over a horizontal line.

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